

**LOW POWER, AREA-EFFICIENT CIRCUIT TO PROVIDE CLOCK
SYNCHRONIZATION**

CROSS-REFERENCE TO RELATED APPLICATION

[00001] The present application claims the benefit of co-pending U.S. Application Serial No. 60/448,760, filed February 20, 2003, by Brent Doyle, entitled: "Low Power, Area-Efficient Circuit to Provide Clock Synchronization," assigned to the assignee of the present application and the disclosure of which is incorporated herein.

FIELD OF THE INVENTION

10 [00002] The present invention relates, in general, to electronic systems and circuits therefor, and is particularly directed to a clock generator circuit for controllably asserting either an internal or an external clock for chip circuitry synchronization.

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BACKGROUND OF THE INVENTION

[00003] Many integrated circuits, such as, but not limited to power management pulse width modulators, employ an

internal clock generator. In some applications it is desirable to override the internally generated clock with an external clock to provide synchronization with other electronics in the system. It is desirable to do this 5 without having to add a ""clock selected" or control" pin to select an internal vs. an external clock, i.e., it is desirable to "sense" the presence of an external clock signal, and use it for the internal clock.

10 **SUMMARY OF THE INVENTION**

[00004] In accordance with the present invention, this objective is readily accomplished by means of a relatively low power, circuit real estate area-efficient, clock signal generator that detects the presence of an externally 15 sourced clock, and then uses this clock as the clock for internal chip circuitry. The present invention is able to provide synchronization from a relatively low frequency range on the order of several Hertz (the lower limit being set by device leakage and size of an electrical energy 20 storage capacitor) to hundreds of MHz (the upper limit being set by gate delays of the fabrication technology employed).

[00005] For this purpose, the present invention comprises a clock steering circuit in the form of a multiplexer having 25 a first input to which an External Clock signal may be applied, and a second input to which an Internal Clock signal is applied. The external clock input port is further

coupled to an inverting delay and to a first input of a logic circuit (e.g., an AND gate or a NAND gate). The output of the inverting delay is coupled to a second input of the logic circuit. The logic circuit has its output
5 coupled to the control input of a switching device. The switching device has a current flow path therethrough coupled to a current source/sink, and in parallel with an electrical energy storage device, in the form of a capacitor that is also coupled to the current source/sink.
10 The connection of the current source/sink and the capacitor is coupled to one input of a comparator, which has a second input coupled to a reference voltage. The output of the comparator is coupled to the select port of the multiplexer. The current supplied by the current source
15 and the value of the capacitor are selected so that the time required for the comparator to reach its trip threshold is defined by $N/f_{\text{internal clock frequency}}$. This allows the circuit to synchronize to an external clock that is as slow as $1/N$ times $f_{\text{internal clock frequency}}$.
20 [00006] In operation, if an external clock having a frequency higher than a prescribed minimum or 'override' frequency is applied to the input port, the controlled switching device will be turned ON sufficiently often, to effectively prevent the capacitor from charging to a
25 voltage value that will trip the comparator. For this 'external override' condition, the output of the comparator will remain in a first logical state, that will cause the

External Clock signal to be coupled by the multiplexer to all chip logic circuitry requiring a clock signal. On the other hand, if no effective external clock is applied to the external clock input port the switching device is never 5 turned on so that the capacitor is not discharged. This allows the voltage across the capacitor to attain a value that will trip the comparator, and change the select input to the multiplexer. In this case, the multiplexer couples the Internal Clock to the clock bus. It may be noted that 10 external clock frequencies above 0 but less than 1/N would be outside the recommended design specification range and would produce an output clock signal that jitters between internal and external clock.

15 **BRIEF DESCRIPTION OF THE DRAWINGS**

[00007] Figure 1 diagrammatically illustrates a circuit for controllably asserting one of an internal clock and an external clock in accordance with a first embodiment of the invention; and

20 [00008] Figure 2 diagrammatically illustrates a circuit for controllably asserting one of an internal clock and an external clock in accordance with a second embodiment of the invention.

25 **DETAILED DESCRIPTION**

[00009] Before describing in detail the new and improved clock generator circuit in accordance with the present

invention, it should be observed that the invention resides primarily in a prescribed modular arrangement of conventional digital circuits and components therefor. In a practical implementation that facilitates their being
5 packaged in a hardware-efficient configuration, this arrangement may be readily implemented as a field programmable gate array (FPGA), or application specific integrated circuit (ASIC) chip set. Consequently, the configuration of such arrangement of circuits and
10 components and the manner in which they are interfaced with other electronic circuitry have, for the most part, been illustrated in the drawings by readily understandable block diagrams, which show only those specific details that are pertinent to the present invention, so as not to obscure
15 the disclosure with details which will be readily apparent to those skilled in the art having the benefit of the description herein. Thus, the block diagram illustrations are primarily intended to show the major components of the invention in a convenient functional grouping, whereby the
20 present invention may be more readily understood.

[00010] Referring now to Figure 1, the architecture of a first embodiment of a clock generator in accordance with the present invention is diagrammatically illustrated as comprising an input port 11, to which an external clock signal denoted External Clock is coupled. Input port is
25 coupled to a first (A0) input port 21 of a 2:1 multiplexer 20, to an inverting delay circuit 30 and to a first input

41 of a logic circuit (e.g., an AND gate) 40. The output of the inverting delay circuit 30 is coupled to a second input 42 of AND gate 40. The output 43 of AND gate 40 is coupled to the control input of a controlled switching device, 5 shown in Figure 1 as the gate input 51 of an N-channel MOSFET 50. Alternatively, switching device 50 may comprise a bipolar transistor or other equivalent component.

[00011] NMOSFET 50 has its drain-source path coupled in parallel with a capacitor 60 and to a current source 70, 10 which sources current from the chip power supply, +V. The source 52 of NMOSFET 50 and one side of the capacitor 60 are coupled to ground, while the drain 53 of NMOSFET 50 and the other side of capacitor 60 are coupled to a first, non-inverting (+) input 81 of a comparator 80 and the current 15 source 70. Comparator 80 has its inverting (-) input 82 coupled to receive a reference voltage VREF and its output 83 coupled to the select (S) input 24 of multiplexer 20. A second input 22 of multiplexer 20 is coupled to the chip's internal clock source that supplies a clock denoted 20 Internal Clock, while the output 23 of multiplexer 20 is coupled to all chip logic circuitry requiring a clock signal. The steering path through multiplexer 20 is such that, for a select input 24 of '0', multiplexer 20 couples its first input 21 (to which the external clock is coupled) 25 to its output port 23, while for a select input 24 of '1', multiplexer 20 couples its second input 22 (to which the internal clock is coupled) to its output port 23.

[00012] Operation of the circuit of Figure 1 is as follows. For the case that an effective external clock is applied to input port 11, then at each rising edge of the external clock (or complementarily, on each falling edge of the external clock, if AND gate 40 is replaced by a NOR gate), NMOSFET 50 is turned ON, discharging capacitor 60, which had been previously been charging by the current supplied from current source 70. As long as the frequency of the external clock signal applied to input port 11 is higher than a prescribed minimum or 'override' frequency, NMOSFET 50 will be turned ON sufficiently often, such that capacitor 60 will not have time to charge up to a value that will allow the voltage at the first input 81 of comparator 80 to rise above the reference voltage VREF.

[00013] As noted briefly above, the current supplied by the current source 70 and the value of capacitor 60 are selected such that the time required for the voltage being supplied to the non-inverting (+) input 81 of comparator 80 is defined by $N/f_{\text{internal clock frequency}}$. This allows synchronization to an external clock that is as slow as $1/N$ times $f_{\text{internal clock frequency}}$. For the 'external override' condition, the output 83 of comparator 80 will remain in a first logical state (e.g., a logical '0') so that the select input 24 of multiplexer 20 remains at that value, causing the External Clock signal, that is coupled from input port 11 to the input 21 of multiplexer 20, to be coupled via its output port 23 to all chip logic circuitry

requiring a clock signal.

[00014] For the case that no effective external clock is applied to the input port 11, the NMOSFET 50 is never turned ON, so that capacitor 60 is not discharged. This 5 will enable the non-inverting (+) input 81 of comparator 80 to increase to a value that exceeds the reference voltage VREF, thereby causing the output 83 of comparator to go high (logical '1'). This, in turn, causes multiplexer 20 to couple the Internal Clock supplied to its input 22 to its 10 output 23 and the system clock bus, as intended.

[00015] Figure 2 diagrammatically illustrates an alternative (complementary) embodiment of the clock selection architecture of Figure 1, where polarities have been reversed. Again, the input port 11, to which the 15 External Clock signal is coupled, is coupled to a first (A0) input port 21 of a 2:1 multiplexer and to an inverting delay circuit 30. The External Clock signal is also coupled to first input 141 of a NAND gate 140. The output of the inverting delay circuit 30 is coupled to a second input 142 of NAND gate 140. The output 143 of NAND gate 140 is coupled to the gate input 151 of a P-channel MOSFET 150. PMOSFET 150 has its drain-source path coupled in parallel with capacitor 60 and to a current sink 170, which is coupled to ground. The source 152 of NMOSFET 150 and one 20 side of the capacitor 60 are coupled to a +V volts voltage rail, while the drain 153 of PMOSFET 150 and the other side of capacitor 60 are coupled to a first, inverting (-) input 25

181 of a comparator 180. Comparator 180 has its non-inverting (+) input 182 coupled to reference voltage VREF and output 183 coupled to the select (S) input 24 of multiplexer 20.

5 [00016] The operation of the complementary polarity version of the invention shown in Figure 2 is essentially the same as that of the embodiment of Figure 1, except that the current source 170 applies a negative current to (or sinks current from) the capacitor 60, which is controllably
10 discharged by NAND gate 140 turning on PMOSFET 150. As in the embodiment of Figure 1, as long as the frequency of the external clock signal is higher than a prescribed minimum 'override' frequency, PMOSFET 150 will be turned ON sufficiently often, such that capacitor 60 will not have
15 time to be charged to a value that will allow the voltage at the first input 181 of comparator 180 to fall below Vref and cause the comparator's output to change state (e.g., 0 to 1), whereby the select input 24 of multiplexer 20 remains at a value that causes the external clock signal at
20 input port 21 to be coupled to its output port 23 and the clock bus.

[00017] On the other hand, if no external clock is applied to input port 11, PMOSFET 150 is never turned ON. This will cause the inverting (-) input 181 of comparator 180 to decrease to a value lower than the reference voltage VREF, thereby causing the output 83 of comparator to go high (logical '1'). Again, as described above, this will cause

multiplexer 20 to couple the Internal Clock supplied to its input 22 to its output 23 and the clock bus, as intended.

[00018] As will be appreciated from the foregoing description, the desire to override an internally generated 5 clock with an external clock to provide synchronization with various electronic circuits of an integrated circuit chip, and without having to add a separate "control" pin to select an internal vs. an external clock, i.e., is successfully addressed by the clock generator circuit of 10 the present invention which, detects the presence of an externally sourced clock, and then couples this clock to the internal chip circuitry. As noted previously, the clock generator of the invention affords synchronization from a relatively low frequency range on the order of several 15 Hertz (the lower limit being set by device leakage and capacitor size) to hundreds of MHz (the upper limit being set by gate delays of the fabrication technology employed).

[00019] While I have shown and described several 20 embodiments in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in the art. I therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and 25 modifications as are obvious to one of ordinary skill in the art.